CoreGEV-Tx10 GigE Vision FPGA IP Core

Transmit uncompressed images over GigE Vision at up to 10 Gbps

Overview

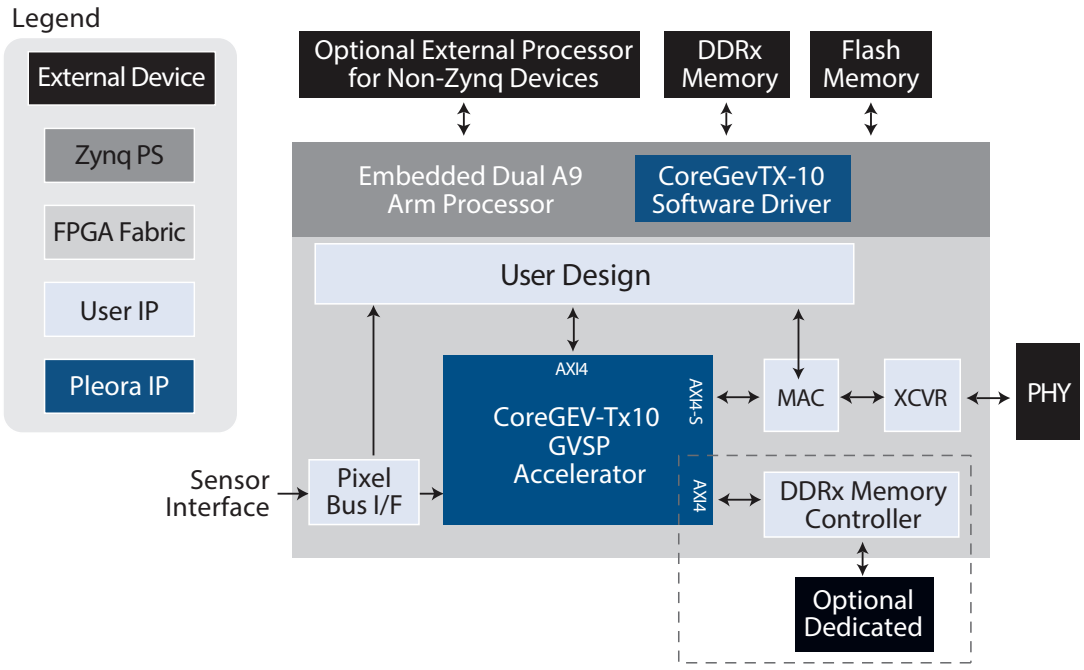
Pleora's **CoreGEV-Tx10 GigE Vision FPGA IP Core** with Flexible Hybrid Accelerator Architecture helps manufacturers shorten time-to- market, reduce risk, and lower costs by providing robust, low latency and high performance GigE Vision®transmit capability for their sensor system.

Pleora's Flexible Hybrid Architecture

- Run full GigE Vision protocol from software-only mode
- Activate CoreGEV driver to allow operation through FPGA for 100% hardware acceleration of GigE Vision for full 10 Gbps throughput
- Get started quicker on designs and implement software from day one in parallel with hardware bring-up
- Firmware allows customer to implement image processing algorithms on a CPU and GPU before transferring to FPGA
- Support for custom GenICam nodes
- Optional dedicated memory interface for highest possible performance

Features

- Supports up to 10 Gbps transmission rates for uncompressed images over standard Ethernet
- Generic AXI ports enable rapid connection to CPU system, memory system, MAC/PHY and video interface
- Low resource utilization for low cost device selection
- Hybrid architecture enabling a fast software-only rapid prototyping mode
- GigE Vision 2.0 compliance ensures interoperability in multi-vendor digital video systems
- GenICam compliant interface provides easy access to programming features and simplifies integration of imaging devices into existing or new systems
- Image management tags an image or group of images with metadata — provides context necessary to retrieve image data from the on-board frame buffer in event of power or network failure at the receiver



GENICAM GIGE VISION

Pleora Technologies

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Hybrid FPGA Accelerator Architecture

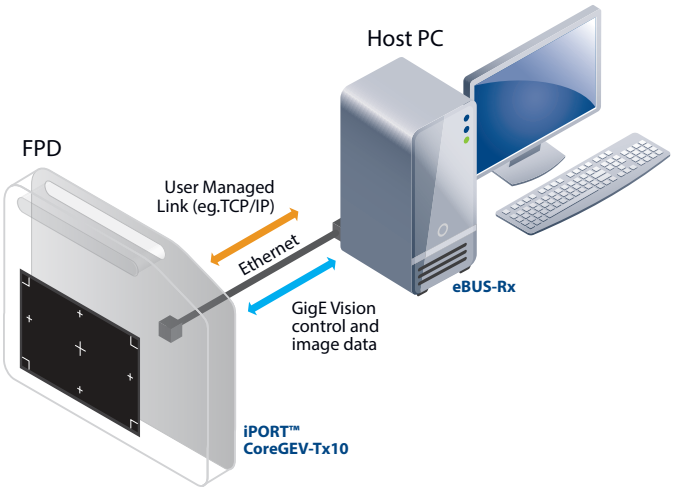
Pleora's unique hybrid FPGA accelerator implementation allows users to bring the sensor up using the onboard processor only and a pure software approach for rapid prototyping. Once the FPGA implementation is complete, users switch the software driver to

"FPGA Acceleration" mode, using the FPGA to offload the video streaming and enabling up to 10 Gbps of low latency transmission of uncompressed images. The software only method can also be used on slower sensors within a family of sensors, reducing development costs and ensuring a consistent interface for software applications across an entire sensor family or families.

The video interface complies with the GigE Vision 2.0 and GenICam™ standards, ensuring interoperability in multi-vendor networked or point-to-point digital video systems. A flexible, dynamically generated, fully customizable GenICam XML file approach allows users to quickly and easily add custom features.

Complete End-to-End Solution

Image streams transmitted by CoreGEV-Tx10 FPGA IP need to be received by the final application, often running on a host PC. Pleora's eBUS™ Software Development Kit (SDK) is a feature-rich application development toolkit providing comprehensive APIs for controlling GigE Vision sensors and for efficiently receive image streams for processing by the host CPU or GPU. By using eBUS, manufacturers can further shorten time to market and development costs for interfacing their end applications to their sensor.



Characteristics	
Pixel Formats	• Mono 8 – 16 bits • For other formats contact Pleora
IEE Tap Geometries (per GenICam SFNC 2.1)	• 1X_1Y • 1X2_1Y • 1X4-1Y • For other tap geometries contact Pleora
Reference Design Sustained Continuous Transmit Rate (Shared memory	• 1.2 Gbps software only mode • 9.2 Gbps accelerator mode
Sensor Interface	AXI4-S interface – allows any custom pixel bus interface to be supported
MAC	User defined, connected via AXI4-S interface. Reference design uses Xilinx 10GE MAC
IEEE 1588	Contact Pleora

Supported Devices	
Reference Design	Zynq-7000
IP Core	RTL supported on Artix-7, Kintex-7, and Virtex-7. Contact Pleora for porting processor software.

Resource Utilization	
LUTs	22K
Registers	18K
BRAM Blocks	40
DSPs	2

Ordering Information	
991-0021	**CoreGEV-Tx10 FPGA IP Core includes** • CoreGEV-Tx10 FPGA Accelerator encrypted RTL design • Hybrid software/hardware accelerator driver • Comprehensive User documentation with quick start guide and tutorials • Sample C++ code for link management • RTL Simulation Testbenches • Fully Compiled Vivado Reference design targeted to Xilinx ZC706 Evaluation Board • eBUS SDK • CoreGEV-Tx10 Hardware Development Kit (906-0005)
906-0005	**CoreGEV-Tx10 Hardware Development Kit (includes all necessary items to start development)** • Xilinx Zynq-7000 SoC ZC706 Evaluation Kit • SD Card preloaded with reference design • Aquantia AQS-107 10G SFP+ 10G BASE-T Module • Intel X550-T1 10G PCIe NIC • First kit is included with IP Core purchase, additional kits can be purchased from Pleora

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